REMARKS

In response to the non-final Official Action of May 12, 2006, minor amendment has been made in the specification to overcome the objections raised by the Office, and claims 1-23 have been canceled with substitution of new claims 24-45. All of these new claims are supported by the original specification and drawings, including Figures 1-5 and the accompanying detailed description at page 14, line 13 through page 19, line 4.

Referring now to the claim objections raised at paragraphs 5 and 6 of the Official Action, appropriate correction has been made in the newly submitted claims.

Referring now to the specification objections raised at paragraphs 7-9 of the Official Action, correction has been made to the specification to correct the typographical errors as noted by the Office.

Referring now to paragraphs 26-28 of the Action, claims 9-11, 15-16 and 20 are rejected under 35 USC §103(a) as unpatentable over US patent 6,898,678, Six et al (hereinafter Six), in view of US patent 6,065,092, Roy. For the reasons set forth below, it is respectfully submitted that newly submitted claim 24, which substantially corresponds to originally presented claim 9, is allowable over said cited art.

More particularly, the present invention as set forth in claim 24 relates to a memory unit having at least two memory areas for storing data. The memory areas may be accessed through two different terminals (first terminals and second terminals). Each of the terminals provides for address ports, control ports, and data ports. The access controllers provide for selectively providing the address and access data through the first and second terminals individually or as a whole through one of the terminals. Thus, the access controllers allow accessing the data either through one of the terminals or through each of the terminals individually.

In the case of sole addressing, one of the terminals accesses memory solely. In this case, the bus-width can be increased for data and thus the clock frequency may be reduced thereby reducing signal integrity issues as set forth in the specification.

Six discloses a digital system having a memory circuit that can be accessed by several requestor circuits. A scheduling circuit is connected to a requestor circuit and is

operable to sequentially schedule memory accesses to the memory circuit (Six, column 1, lines 59-65). There is provided a sequential access by the requestor circuits, as well as exclusive access by requestor circuits (Six, column 2, lines 1-6). Six describes two access modes, which are shared access and host only access (Six, column 3, lines 24-36). Access to memory banks is provided through first in, first out (FIFO) ports which are operated independently of each other and provide independent data transfer (Six, column 6, lines 24-54).

Roy provides for accessing memory with at least two multi-line channels using different accessing modes, such as cooperative mode and synchronous mode (Roy, column 7, lines 10-49). In cooperative mode, address and control information are provided through one channel and data is provided through another channel; whereas in synchronous mode, control and address information and data are provided through at least two channels.

The Office asserts at paragraph 28 of the Official Action that Six discloses a memory unit of claim 1 but does not disclose expressly "receiving access signals solely through one terminal and providing data from memory areas through both terminals, or receiving access signals and providing data from memory areas through both terminals individually, respectively." The Office further asserts that Roy discloses the concept of "receiving access signals solely through one terminal and providing data from memory areas through both terminals, or receiving access signals and providing data from memory areas through both terminals individually, respectively."

It is respectfully submitted that the Office neglects to consider the fact that according to the features recited in claim 24, in case of sole addressing and accessing data, the access controllers provide access to the memory area by control ports and address ports of one of the first and second terminals and provides the data through data ports of both of said first and second terminals. This statement in claim 24 requires that each of the first and second terminals has control ports, address ports and data ports, which are therefore separated from each other. It is respectfully submitted that the Office interprets these requirements of claim 24 as receiving address signals and providing data from memory areas through both terminals individually, respectively.

The Office is therefore of the opinion that receiving signals solely through one terminal and providing data from memory areas through both terminals would be known.

However, according to Roy, each channel provides on the same lines both data and address information (Roy, column 7, lines 26-29 and column 9, lines 11-14). However, the present invention as claimed in claim 24 provides for first and second terminals which have, separated from each other, control ports, address ports and data ports. The sole addressing mode according to the present invention provides for accessing data through data ports of both terminals using control and address ports of only one of the terminals. This feature of claim 24 is not possible according to Roy since Roy does not provide for accessing data through control and address ports which are different than the data ports. Therefore, it is respectfully submitted that the requirements of claim 24 are not obvious in view of Six, further in view of Roy.

Since claim 24 is believed to be distinguished over the cited art, it is respectfully submitted that claims 25-40, all of which ultimately depend from claim 24, are further distinguished over the cited art.

Method claim 41 recites actions corresponding to the memory unit recited in claim 24 and, for similar reasons, it is believed to be distinguished over the cited art.

Similarly, system claim 42 recites first and second processors and at least two access controllers having features corresponding to claim 24. As such, system claim 42 is also believed to be distinguished over the cited art.

Module claim 43 and mobile communication device claim 44 depend from claim 24 and are therefore also believed to be distinguished over the cited art.

Newly submitted claim 45 recites a memory unit in which the elements are presented in a means-plus-function format. This claim is similar to claim 24. As such, claim 45 and claim 46, dependent thereon, are believed to be distinguished over the cited art.

It should further be noted that the recitation of access controller in the claims is supported by the original specification and drawings, including the state machines (20) shown in Figure 2 and the corresponding description thereof in the specification, including page 11, lines 6-18.

In view of the foregoing, it is respectfully submitted that the present application as amended is in condition for allowance and such action is earnestly solicited.

Respectfully submitted,

Dated: October 12, 2006

Alfred A. Fressola
Attorney for Applicants
Registration No. 27,550

WARE, FRESSOLA, VAN DER
SLUYS & ADOLPHSON LLP
Building Five, Bradford Green
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955